

PATENT APPLICATION

042390.P12397

Amendment to Claims

Please cancel claims 14-21, without prejudice, as shown below.

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1. (Original) A non-volatile memory package comprising:
a substrate having a first surface and a second surface;
an integrated circuit die including a memory array mounted to the first surface of
the substrate; and
a passive component mounted to the second surface of the substrate.
2. (Original) The non-volatile memory package of claim 1, wherein the passive
component is electrically coupled to the integrated circuit die.
3. (Original) The non-volatile memory package of claim 1, further comprising an
array of solder balls mounted to the substrate.
4. (Original) The non-volatile memory package of claim 3, wherein the passive
component is located centrally within the array of solder balls.
5. (Original) The non-volatile memory package of claim 4, wherein the passive
component has a height less than a height of the solder balls.

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6. (Original) The non-volatile memory package of claim 1, wherein the passive component is at least a portion of a voltage regulator circuit coupled to the integrated circuit die.

7. (Original) The non-volatile memory package of claim 1, wherein the substrate comprises a cavity and at least a portion of the passive component lies within the cavity.

8. (Original) The non-volatile memory package of claim 7, further comprising an array of solder balls mounted to the substrate, wherein the passive component has a height less than a height of the solder balls.

9.
10. (Original) The non-volatile memory package of claim 1, wherein the passive component is mounted to the second surface of the substrate with an epoxy material.

10.
11. (Original) The non-volatile memory package of claim 9, wherein the epoxy material between the passive component and the substrate is less than about 0.1 millimeters in thickness.

11.
12. (Original) The non-volatile memory package of claim 1, wherein the passive component is mounted to the substrate with a conductive material.

12.
13. (Original) The non-volatile memory package of claim 1, wherein the passive component includes a capacitor or an inductor.

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~~14~~. (Original) The memory device of claim 1, wherein the integrated circuit die includes a flash memory array.

¹⁴
~~14~~.

~~13~~. (Cancelled) A method comprising:

forming a substrate;

mounting an integrated circuit die on said substrate;

mounting a passive component overly the substrate; and

electrically coupling the passive component to at least a portion of the integrated circuit die.

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~~15~~.

~~14~~. (Cancelled) The method of claim ¹²~~13~~, further comprising adhesively attaching the passive component to he integrated circuit die.

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~~16~~.

~~15~~. (Cancelled) The method of claim ¹³~~14~~, further comprising adhesively attaching the passive component to the integrated circuit die with a non-conductive adhesive.

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~~16~~. (Cancelled) The method of claim ¹²~~15~~ including wire bonding the passive component to the substrate.

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~~18~~.

~~17~~. (Cancelled) The method of claim ¹²~~16~~ including wire bonding the passive component to the integrated circuit die.

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^{19.}

~~18.~~ (Cancelled) A method comprising:

molding an integrated circuit die and at least one passive component to a voltage regulator circuit into a package, the integrated circuit die including a non-volatile memory array.

^{20.}

~~18.~~ (Cancelled) The method of claim ¹⁹~~18~~, further comprising mounting the at least one passive component to the integrated circuit die.

^{21.}

~~20.~~ (Cancelled) The method of claim ¹⁹~~18~~, further comprising forming a wire bond to electrically couple the at least one passive component and the integrated circuit.
